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Influence of the local trapped charge in oxide to the gate - drain capacitance in a finFET

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Abstract: In this paper, the influence of the local trapped charge in the gate oxide layer on the total of the capacity of gate-drain is studied. It was investigated that the approaching of the local trapped charge in the gate oxide layer towards the source influences the change in the density of electrons and holes in the drain-channel regions and electric capacity of drain-channel regions.

Key words: trapped charge, oxide-semiconductor region, density of electrons and holes, p-n junction, electric capacity, gate, drain and channel.

Аннотация: В данной работе исследуется влияние локальизованного заряда в оксидном слое затвора на емкость затвор-сток. Показано, что с приближением локального заряда в оксидном слое к истоку влияет на изменение плотности электронов и дырок в областях сток-канал и емкость областей сток-канал.

Ключевые слова: локального заряд, оксидно-полупроводниковая область, плотность электронов и дырок, p-n переход, электрическая емкость, затвор, сток и канал.

Annotatsiya: Ushbu maqolada biz zatvor ostidagi oksid qatlamidagi qamralgan zaryadning zatvor-stok sig'imiga ta'sirini o'rganamiz. Ko'rsatilgandek, oksid qatlamidagi qamralgan zaryad istokga yaqinlashganda, u stok-kanal soxalaridagi elektronlar va kovaklarning zichligi va stok-kanal soxalari sig'imining o'zgarishiga ta'sir qiladi.

Kalit so'zlar: Qamralgan zaryad, oksid va yarimo'tkazgich soxasi, elektronlar va kovaklar zichligi, p-n o'tish, elektr sig'imi, zatvor stok, kanal.

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I. Introduction

At the semiconductor-oxide interface in a metal-oxide semiconductor stack, imperfections in the chemical structure lead to interface traps. These localized defects can trap and release mobile charge, leading to drain-current noise [1-2] as well as a reduced electrostatic control of the gate over the channel [3-5]. Interface traps are formed during device processing, but can be additionally created by e.g. ionizing radiation and electrical stress. CMOS process development, process control and reliability assessment require an accurate estimate of the interface state density in these devices. Trapped charges can have a significant impact on the capacitance between the gate and the source layers in FinFETs. Trapped charges can cause a shift in the threshold voltage, which can affect the device's performance, and can also alter the effective capacitance between the gate and the source layers [6]. When charges are trapped in the gate oxide layer of a FinFET, they can alter the effective thickness of the oxide layer, which affects the capacitance between the gate and the source layers. The trapped charges can act as additional charges that contribute to the capacitance between the gate and the source, and can increase or decrease the effective capacitance depending on their polarity and density. Moreover, the presence of trapped charges can also alter the threshold voltage of the device. The trapped charges can create an electric field that opposes the gate electric field, leading to a shift in the threshold voltage. This shift in the threshold voltage can cause the device to operate at a higher or lower voltage than intended, which can result in performance issues. To mitigate the effects of trapped charges on the capacitance between the gate and the source layers, various techniques may be used, such as incorporating a high-k dielectric material to reduce the density of trapped charges, or using a gate stack engineering technique to reduce the effective thickness of the oxide layer[7]. Additionally, annealing or bias-stress techniques may also be employed to reduce the impact of trapped charges on the device's performance. Annealing is a process that involves heating the FinFET device to a high temperature for a short period of

time. Annealing can help to reduce the effects of trapped charges on the capacitance between the gate and the source layers. During the annealing process, the trapped charges can be neutralized or redistributed, which can reduce their impact on the device's performance. Bias-stress techniques involve applying a voltage bias to the gate of the FinFET for an extended period of time. The application of the bias voltage can cause the trapped charges to move, and the effect of the trapped charges on the device's performance can be measured[8]. By studying the effects of the bias voltage, the impact of trapped charges on the device's performance can be characterized, and steps can be taken to mitigate their effects. Trapped charges can significantly impact the capacitance between the gate and the source layers in FinFETs. The presence of trapped charges can alter the effective thickness of the gate oxide layer, which affects the capacitance between the gate and the source layers. Additionally, trapped charges can also shift the threshold voltage of the device, leading to performance issues. Various techniques such as high-k dielectric material, gate stack engineering, annealing, and bias-stress techniques can be used to mitigate the effects of trapped charges on the device's performance [9]. Nowadays, studying the influence of the accumulated charges in the defects of the gate oxide region via the long-time operation of FinFET is one of the actual problems. The purpose of this paper is to study the influence of the local accumulated charge in the gate oxide layer on the capacitance of gate-drain.

II. Device structure and simulation conditions

In our research 3D-modeling was carried out using the Advanced TCAD Sentaurus program [10]. The structure of the FinFET studied in this paper by of the simulation is shown in Fig. 1. A diffusion-drift transport model was used in the simulation. The model takes into account the Shockley–Read–Hall recombination and Auger recombination for minority carriers. The mobility model doping dependence and velocity saturation was also included. Since the transistor has a nanometer size, it is necessary to take into account the quantum effects. The most preferred for diffusiondrift simulation is the density gradient quantum correction [11], which was used in this study. The model was calibrated according to the experimental results (Fig. 2) [12].

Fig. 1. The structure of the FinFET studied by of the simulation

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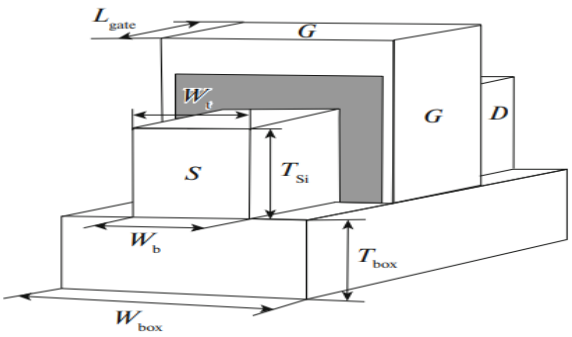

Fig. 1. The structure of the FinFET studied by of the simulation

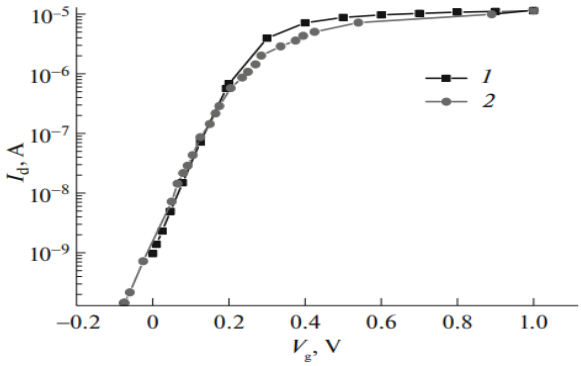

Fig. 2. Calibration of the I–V characteristic of (1) a simulated transistor by (2) experimental results of at L_{gate} = 25 nm and V_{ds} = 50 mV.

The following structure parameters were used in the simulation. The length of the polysilicon gate (G) doped with phosphorus at a concentration of 10^{20} cm^{-3} is L_{gate} = 25 nm. HfO_2 with an equivalent thickness of t_{ox} = 0.35 nm is taken as a gate oxide layer. The length and width of the buried oxide layer were L_{box} = 75 nm and W_{box} = 100 nm, respectively. The transistor fin is doped with boron at a concentration of 10^{15} cm^{-3}, has the height T_{si}=30 nm and a base width of W_b = 12 nm, the drain (D) and source (S) regions are doped with phosphorus with a Gaussian profile with a maximal concentration of 10^{20} cm^{-3}. The lengths of the drain and source regions are 25 nm. For study influence the trapped charges in semiconductor-insulator interface to the capacitance between the gate and the source layers. In simulation charged layer has set as fig.3. At here width of charged layer is 5 nm which as shown Fig. 3. Volume bulk density of charge is equal to $4 \cdot 10^{18}$ C/m^3.

III. Simulations results and discussion

In the simulation, the charged layer moves from drain to source with 5nm step by step as shown Fig. 3. Besides, in the second stage the charged region extended from 5nm to 25 nm step by step. In simulation, the change in capacitance between the gate

and the drain was studied when the charged gate oxide region moved from the drain to the source when the drain was supplied with a voltage of 5 V. The obtained results are presented in Fig. 4.

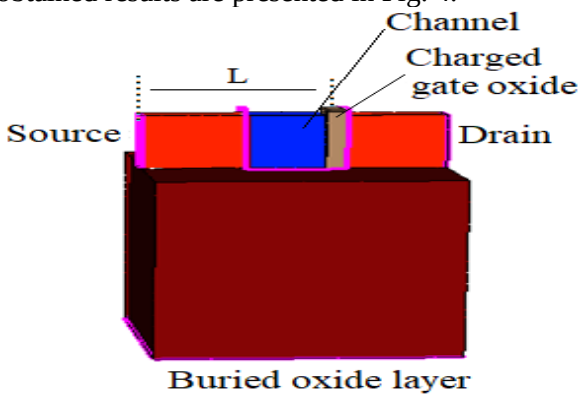

Fig. 3. Location of charged gate oxide region and its moving from drain to source with 5nm step.

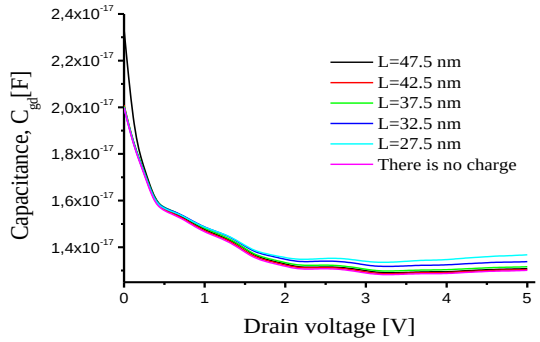

Fig. 4. The change capacitance between the gate and the drain depending on the located distance of charged gate oxide region

The analysis of the results obtained in Fig. 4. indicates that, there is impact of the local charged region on the gate-drain electric capacity. The change of the gate-drain electric capacity depends on the change of the p-n junction capacity. Because the charged region influences to the depletion region in the p-n junction. For to determine this, we will check the influence of the charged region on the density of electrons and holes in the p-n junction. The obtained results are presented in Fig. 5. and Fig. 6.

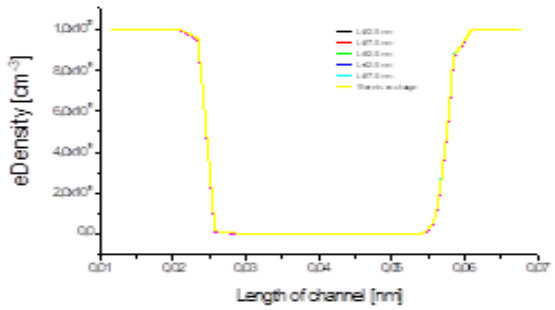

Fig.5. Electron density along the channel 1 nm below the top of the channel

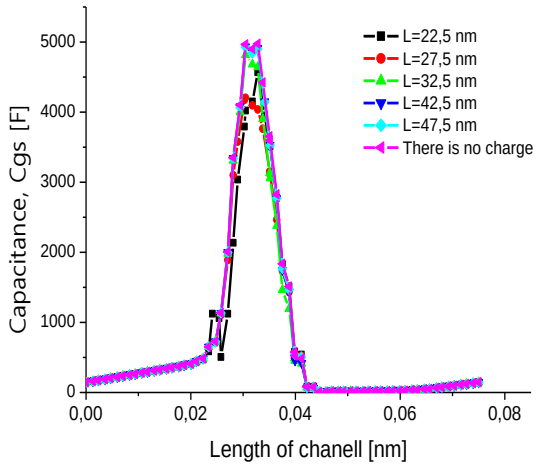

Fig.6. Hole density along the channel 1 nm below the top of the channel

If we analyze the obtained results, the approaching of the charged region to the source side causes a change in the density of electrons and holes in the p-n junction region. we can see it from Fig. 5. and Fig. 6. It is the change in the density of electrons and holes that changes the electric capacity of the p-n junction. If the capacitance of the p-n junction changes, the total capacitance of between the gate and drain also changes. But the influence on the total electrical capacity of gate-drain is less than that of the p-n junction electrical capacity. Because the total capacitance of the gate-drain is formed by the series connection capacitance of metal-oxide, capacitance of oxide-semiconductor and capacitance of p-n junction. In this paper, the investigate of the thickness of the gate oxide layer on the capacity of gate-drain is also studied. In simulation prosses, the capacity of drain-gate was calculated in the thickness of the HfO_2 oxide layer from 2 nm to 3.5 nm. The obtained results and the equivalent structure of the vertical field-effect transistor (FinFET) studied in the simulation are shown in Fig. 7. and Fig. 8.

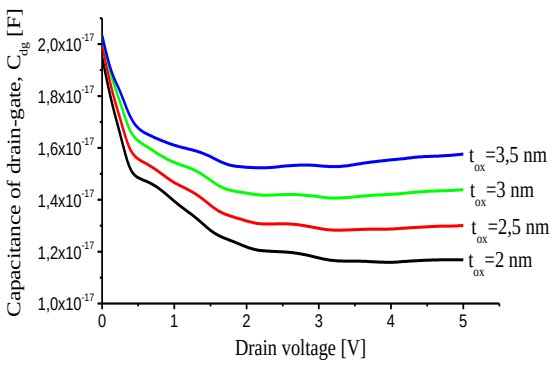

Fig.7. Impact of oxide layer thickness on capacitance of drain-gate

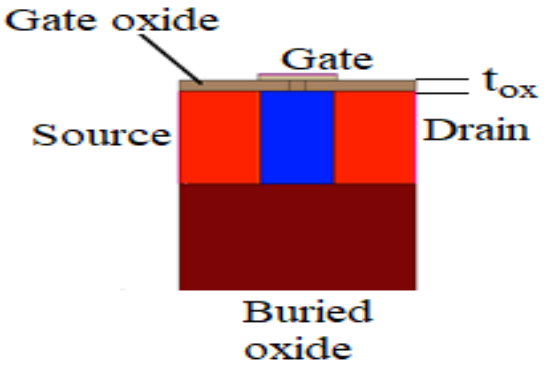

Fig. 8. Equivalent structure of the vertical field-effect transistor.

IV. Conclusion

Using the obtained results and their discussion can be give as follow main conclusions. The trapped charge at the gate oxide influences the density of electrons, holes in the drain-channel region and capacitance of the p-n junction in the drain-channel region. The approaching of the trapped charge to the source has a stronger influence on the electric capacity of the p-n junction in the drain-channel region. It was determined that the capacitance of drain-gate increases when the thickness of the oxide layer increases.

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Theme of article: Influence of the local trapped charge in oxide to the gate - drain capacitance in a finFET

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